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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/505,949	02/15/2000	Michael Chow	042390.P6447	5605
7590	12/14/2004			EXAMINER
Thomas M Coester Blakely Sokoloff Taylor and Zafman LLP 12400 Wilshire Boulevard Seventh Floor Los Angeles, CA 90025			Li, AIMEE J	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/505,949	CHOW ET AL. <i>CH</i>
Examiner	Art Unit	
Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 03 September 2004.  
 2a) This action is FINAL.                            2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-19 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-19 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_

5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_

**DETAILED ACTION**

1. Claims 1-19 have been considered.
2. In view of the Appeal Brief filed on 03 September 2004, PROSECUTION IS HEREBY REOPENED. The rejections are set forth below.
3. To avoid abandonment of the application, appellant must exercise one of the following two options:
  - (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,
  - (2) request reinstatement of the appeal.
4. If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 7-13, and 15-19 rejected under 35 U.S.C. 102(b) as being taught by Blomgren et al., U.S. Patent Number 5,685,009 (herein referred to as '009), and U.S. Patent Number 5,781,750 (herein referred to as '750) incorporated by reference into '009 at column 3, lines 44-47. The shared registers disclosed in '009 are for use in the device disclosed in '750, as

shown in '009 in column 1, line 24 to column 2, line 33; column 3, lines 444-67; and column 4, lines 6-16, hence '750 is incorporated by reference in '009 in the same embodiment.

7. Referring to claim 1, '009 and '750 have taught a processor comprising:

- a. A first instruction set engine to process instructions from a first instruction set architecture (ISA) having a first word size ('009 column 1, lines 24-33 and 44-48 and column 1, line 59 to column 2, line 4; and '750 Abstract; column 3, lines 51-55 and 59-65; column 6, lines 16-24; and Figure 2). In regards to '009 and '750, it is inherent that the two ISAs are different sizes, since RISC, specifically the x86 instruction set, and CISC, specifically the PowerPC instruction set, are different word sizes. For more information please see the provided information for more information on the x86 and PowerPC instruction sets and Heuring and Jordan's Computer Systems Design and Architecture provided with the action dated 18 June 2003 about the RISC and CISC instruction sets.
- b. A second instruction set engine to process instructions from a second ISA having a second word size, the second word size being different than the first word size ('009 column 1, lines 24-33 and 44-48 and column 1, line 59 to column 2, line 4; and '750 Abstract; column 3, lines 51-55 and 59-65; column 6, lines 16-24; and Figure 2). In regards to '009 and '750, it is inherent that the two ISAs are different sizes, since RISC, specifically the x86 instruction set, and CISC, specifically the PowerPC instruction set, are different word sizes. For more information please see the provided information for more information on the x86 and PowerPC instruction sets and Heuring and Jordan's Computer Systems

Design and Architecture provided with the action dated 18 June 2003 about the RISC and CISC instruction sets.

- c. A mode identifier ('750 Abstract; column 3, line 65 to column 4, line 2; column 4, lines 7-11; column 6, lines 53-57; and Figure 2);
- d. A plurality of floating-point registers shared by the first instruction set engine and the second instruction set engine ('009 column 2, lines 13-16; column 2, lines 41-58; column 10, lines 43-53; column 18, lines 3-16; column 19, lines 47-48; column 20, lines 10-15; Figures 6-8); and
- e. A floating-point unit coupled to the floating-point registers, the floating-point unit processing an input responsive to the mode identifier to produce an output ('009 column 22, lines 48-54; and '750 column 3, line 65 to column 4, line 2; column 4, lines 7-11; column 6, lines 53-57; column 7, lines 1-12; and Figure 2 ).

8. Referring to claim 2, '009 and '750 have taught wherein the mode identifier is one of a plurality of bits in a processor status register ('750 Abstract; column 3, line 65 to column 4, line 2; column 4, lines 7-11; column 6, lines 53-57; and Figure 2).

9. Referring to claim 3, '009 and '750 have taught wherein the floating-point unit comprises:

- a. Pre-processing hardware to detect if a token exists in the input ('009 column 1, lines 43-47 and column 2, lines 51-58; and '750 column 3, line 65 to column 4, line 21; column 6, lines 53-59; column 7, lines 30-54; and Figure 2);
- b. An arithmetic unit responsive to the input and the mode identifier ('009 column 1, lines 43-47; and '750 column 6, line 53 to column 7, line 12; and Figure 2); and

- c. Post-processing hardware to perform a token specific operation if a token exists in the input ('009 column 3, lines 57-67; and '750 column 5, line 49 to column 6, line 13).

10. Referring to claim 4, '009 and '750 have taught wherein the input includes data stored in at least one of the floating-point registers ('009 column 4, lines 17-34; column 9, lines 21-28; column 18, lines 3-16; column 19, lines 47-48; column 20, lines 10-15; and Figures 7-8).

11. Referring to claim 5, '009 and '750 have taught wherein the input may contain a token ('009 column 1, lines 43-47 and column 2, lines 51-58; and '750 column 3, line 65 to column 4, line 21; column 6, lines 53-59; column 7, lines 30-54; and Figure 2), wherein the floating-point registers are 82 bits wide ('009 column 2, lines 13-22), and wherein the token being an 82 bit processor known value ('009 column 1, lines 43-47 and column 2, lines 13-22 and 51-58; and '750 column 3, line 65 to column 4, line 21; column 6, lines 53-59; column 7, lines 30-54; and Figure 2).

12. Referring to claim 7, '009 and '750 have taught wherein the floating point registers each comprise

- a. A sign bit ('009 column 2, lines 12-22). In regard to '009, it is inherent that the significand, also known as the mantissa, includes the sign bit. Please see FOLDOC definition mantissa ©1996 provided with the Office Action dated 30 June 2003.
- b. An exponent ('009 column 2, lines 12-22); and
- c. A significand ('009 column 2, lines 12-22). In regards to '009, it is inherent and well-known in the art that a significand is the same as the mantissa. Please see

David Goldberg's "What Every Computer Scientist Should Know About Floating-point Arithmetic" ©1991, specifically under the section titled "Floating-point Formats", paragraph 2 "where  $d.dd\dots d$  is called the *significand*" which refers to footnote 2 which says "This term was introduced by Forsythe and Moler [1967], and has generally replaced the older term *mantissa*."

13. Referring to claim 8, '009 and '750 have taught wherein the mode identifier indicates whether the processor is in a first mode or a second mode ('750 Abstract; column 3, line 65 to column 4, line 2; column 4, lines 7-11; column 6, lines 53-57; and Figure 2).

14. Referring to claim 9, '009 and '750 have taught wherein the mode identifier indicates whether the processor is in a 32 bit word ISA mode or a 64 bit word ISA mode ('009 column 1, lines 24-33 and 44-48 and column 1, line 59 to column 2, line 4; and '750 Abstract; column 3, lines 51-55 and 59-65; column 6, lines 16-24; and Figure 2). In regards to '009 and '750, the PowerPC instruction mode, i.e. RISC instruction mode, has 32 bit instruction words, as is the nature of the PowerPC instruction set. The x instruction mode, i.e. CISC instruction mode, has variable length instructions, which includes the 64-bit instruction length. For more information please see the provided information for more information on the x86 and PowerPC instruction sets and Heuring and Jordan's Computer Systems Design and Architecture provided with the action dated 18 June 2003 about the RISC and CISC instruction sets.

15. Referring to claim 10, '009 and '750 have taught a method in a processor comprising:

a. Fetching an input from at least one of a plurality of floating-point registers ('009 column 2, lines 13-16; column 2, lines 41-58; column 10, lines 43-53; column 18, lines 3-16; column 19, lines 47-48; column 20, lines 10-15; Figures 6-8);

- b. Detecting whether the input includes a token ('009 column 1, lines 43-47 and column 2, lines 51-58; and '750 column 3, line 65 to column 4, line 21; column 6, lines 53-59; column 7, lines 30-54; and Figure 2);  
c. If the token is detected in the input, checking what mode the processor is in ('009 column 1, lines 43-47 and column 2, lines 51-58; and '750 column 3, line 65 to column 4, line 21; column 6, lines 53-59; column 7, lines 30-54; and Figure 2);  
d. If the processor is in a first mode, processing the input to render an arithmetic result ('009 column 1, lines 43-47; and '750 column 6, line 53 to column 7, line 12; and Figure 2);  
e. If the processor is in a second mode, performing a token specific operation ('009 column 3, lines 57-67; and '750 column 5, line 49 to column 6, line 13); and  
f. Producing an output ('009 column 1, lines 43-47 and column 3, lines 57-67; and '750 column 5, line 49 to column 6, line 13; column 6, line 53 to column 7, line 12; and Figure 2).
16. Referring to claim 11, '009 and '750 has taught
  - a. Wherein the input is comprised of at least one operand and at least one operator ('750 column 3, lines 51-56). In regards to '750, the PowerPC RISC instruction set and x86 CISC instruction set both have at least one operand and at least one operator. Please see the provided information on the PowerPC and x86 instruction sets.
  - b. Wherein detecting comprises examining the at least one operand to determine whether any of the operands correspond to the token ('009 column 1, lines 43-47

and column 2, lines 51-58; and '750 column 3, line 65 to column 4, line 21;

column 6, lines 53-59; column 7, lines 30-54; and Figure 2); and

- c. Wherein checking comprises examining a mode identifier to determine whether the processor is in the first mode or the second mode ('009 column 1, lines 43-47 and column 2, lines 51-58; and '750 column 3, line 65 to column 4, line 21; column 6, lines 53-59; column 7, lines 30-54; and Figure 2).

17. Referring to claim 12, '009 and '750 have taught wherein processing comprises executing at least one operation on the at least one operand according to the at least one operator to achieve a result ('009 column 1, lines 43-47; and '750 column 6, line 53 to column 7, line 12; and Figure 2).

18. Referring to claim 13, '009 and '750 have taught wherein performing comprises propagating the token ('009 column 3, lines 57-67; and '750 column 5, line 49 to column 6, line 13); and wherein producing output comprises setting the output to be the token ('009 column 3, lines 57-67; and '750 column 5, line 49 to column 6, line 13). In regards to '009 and '750, the indication that the CPU is in emulation mode must be propagated through the entire process of switching from CISC to RISC and back to CISC.

19. Referring to claim 15, '009 and '750 have taught wherein checking comprises checking a mode identifier ('009 column 1, lines 43-47 and column 2, lines 51-58; and '750 column 3, line 65 to column 4, line 21; column 6, lines 53-59; column 7, lines 30-54; and Figure 2).

20. Referring to claim 16, '009 and '750 have taught wherein checking comprises checking a mode identifier bit in a processor status register ('009 column 1, lines 43-47 and column 2, lines

51-58; and '750 column 3, line 65 to column 4, line 21; column 6, lines 53-59; column 7, lines 30-54; and Figure 2).

21. Referring to claim 17, '009 and '750 have taught wherein the first mode is a 32 bit word ISA mode and the second mode is a 64 bit word ISA mode ('009 column 1, lines 24-33 and 44-48 and column 1, line 59 to column 2, line 4; and '750 Abstract; column 3, lines 51-55 and 59-65; column 6, lines 16-24; and Figure 2). In regards to '009 and '750, the PowerPC instruction mode, i.e. RISC instruction mode, has 32 bit instruction words, as is the nature of the PowerPC instruction set. The x instruction mode, i.e. CISC instruction mode, has variable length instructions, which includes the 64-bit instruction length. For more information please see the provided information for more information on the x86 and PowerPC instruction sets and Heuring and Jordan's Computer Systems Design and Architecture provided with the action dated 18 June 2003 about the RISC and CISC instruction sets.

22. Referring to claim 19, '009 and '750 have taught a method in a multi-mode processor comprising:

- a. Fetching an input from at least one of a plurality of floating-point registers ('009 column 2, lines 13-16; column 2, lines 41-58; column 10, lines 43-53; column 18, lines 3-16; column 19, lines 47-48; column 20, lines 10-15; Figures 6-8);
- b. Detecting whether the input includes at least one token of a plurality of tokens ('009 column 1, lines 43-47 and column 2, lines 51-58; and '750 column 3, line 65 to column 4, line 21; column 6, lines 53-59; column 7, lines 30-54; and Figure 2);

- c. If at least one token is detected in the input, checking what mode the processor is in ('009 column 1, lines 43-47 and column 2, lines 51-58; and '750 column 3, line 65 to column 4, line 21; column 6, lines 53-59; column 7, lines 30-54; and Figure 2);
- d. Processing the input to render an arithmetic result when the processor is in at least a first mode of a plurality of modes ('009 column 1, lines 43-47; and '750 column 6, line 53 to column 7, line 12; and Figure 2); and
- e. Performing a token specific operation when the processor is in at least a second mode of a plurality of modes ('009 column 3, lines 57-67; and '750 column 5, line 49 to column 6, line 13).

***Claim Rejections - 35 USC § 103***

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

24. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren et al., U.S. Patent Number 5,685,009 (herein referred to as '009), and U.S. Patent Number 5,781,750 (herein referred to as '750) incorporated by reference into '009 at column 3, lines 44-47 in view of InstantWeb's Online Computing Dictionary terms "speculative evaluation" and "speculative execution" (herein referred to as FOLDOC). '009 and '750 have taught wherein the token represents a "not a thing value" (NaTVal) that defines an unsuccessful load request ('750 column 4, lines 13-33 and column 7, lines 25-32). In regards to '750, the TLB

is used to load the physical address of the instruction when virtual addresses are present and emulation mode is entered when a miss occurs in the TLB, i.e. cannot find the physical address to load, thereby creating an unsuccessful load request. FOLDOC has taught speculative evaluation and execution of instructions (FOLDOC terms “speculative evaluation” and “speculative execution”). A person of ordinary skill in the art at the time the invention was made would have recognized that speculative evaluation and execution reduces the overall run-time of a process and keeps all functional units working, i.e. not wasted cycles, (FOLDOC terms “speculative evaluation” and “speculative execution”), thereby increasing processor speed and efficiency. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the speculative evaluation and execution of FOLDOC in the device of ‘009 and ‘750 to improve processor speed and efficiency.

25. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren et al., U.S. Patent Number 5,685,009 (herein referred to as ‘009), and U.S. Patent Number 5,781,750 (herein referred to as ‘750) incorporated by reference into ‘009 at column 3, lines 44-47 in view of Amos Omondi’s The Microarchitecture of Pipelined and Superscalar Computers ©1999 (herein referred to as Omondi). ‘009 and ‘750 have taught a multi-mode processor comprising:

- a. A plurality of instruction set engines to process instructions from a plurality of instruction set architectures having different word sizes (‘009 column 1, lines 24-33 and 44-48 and column 1, line 59 to column 2, line 4; and ‘750 Abstract; column 3, lines 51-55 and 59-65; column 6, lines 16-24; and Figure 2). In regards to ‘009 and ‘750, it is inherent that the two ISAs are different sizes, since RISC, specifically the x86 instruction set, and CISC, specifically the PowerPC

instruction set, are different word sizes. For more information please see the provided information for more information on the x86 and PowerPC instruction sets and Heuring and Jordan's Computer Systems Design and Architecture provided with the action dated 18 June 2003 about the RISC and CISC instruction sets.;

- b. A mode identifier ('750 Abstract; column 3, line 65 to column 4, line 2; column 4, lines 7-11; column 6, lines 53-57; and Figure 2);
- c. A plurality of floating-point registers shared by the instruction set engines ('009 column 2, lines 13-16; column 2, lines 41-58; column 10, lines 43-53; column 18, lines 3-16; column 19, lines 47-48; column 20, lines 10-15; Figures 6-8); and
- d. A floating-point unit coupled to the floating-point registers, the floating-point units processing an input responsive to the mode identifier ('009 column 22, lines 48-54; and '750 column 3, line 65 to column 4, line 2; column 4, lines 7-11; column 6, lines 53-57; column 7, lines 1-12; and Figure 2).

26. '009 and '750 have not explicitly taught a plurality of floating-point units. Omondi has taught a plurality of floating-point units (Omondi Figure 1.9; Figure 1.11; Figure 1.12; and Figure 1.13). A person of ordinary skill in the art at the time the invention was made would have recognized that a superscalar processor, such as those shown in Omondi, execute more than one instruction at a time, thereby increasing the speed and efficiency of a processor (Omondi page 6, section 1.3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the superscalar processor of Omondi in the device of '009 and '750 to increase the speed and efficiency of the processor. Also, merely duplicating a

part of a device for multiple effect is not a patentable difference, see *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

***Response to Arguments***

27. Applicant's arguments, see Supplemental Appeal Brief, filed 03 September 2004, with respect to the rejection(s) of claim(s) 1-19 under 35 U.S.C. § 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the above.

***Conclusion***

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

- a. Paul Demone's "RISC vs. CISC Still Matters" ©13 February 2000 has taught the difference between RISC and CISC instruction sets, including the different instruction word sizes, and has exemplified of each type of instruction set, including the PowerPC for RISC and x86 family for CISC.
- b. Bob Ryan's "NexGen Nx586 Straddles the RISC/CISC Divide" ©June 1994 has taught a processor with RISC and CISC properties.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL  
Aimee J. Li  
8 December 2004

*Eddie Chan*  
EDDIE CHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100